What is claimed is:

1. A storage disk, comprising:

a plurality of sectors positioned on a surface of the storage disk so as to be read by a storage device, each sector having a header section and a data section;

wherein the header section comprises a plurality of address blocks, each address block containing an address mark followed by an address field, each address field within a sector having the same address data coded in a biphase format for identifying sector address, each address mark being distinguishable from the biphase coded address data.

2. The storage disk of claim 1 wherein the plurality of sectors are positioned on adjacent land and groove tracks and the respective address sections are repeated alternately on the land track and groove tracks in a checkerboard format.

3. The storage disk of claim 1 wherein the address data is sampled with an asynchronous clock.

4. The storage disk of claim 3 wherein the address data includes a predetermined number of data bits with each data bit being a predetermined number of channel bits long, wherein each data bit includes a mark-space or space-mark transition at a predetermined location.

5. The storage disk of claim 4 wherein the address data is six channel bits long and includes a 3T mark and a 3T space.

6. The storage disk of claim 1 wherein the address data is embossed.

7. The storage disk of claim 1 wherein the address section further includes an error detection field.

8. The storage disk of claim 5 wherein the address mark is made up of marks and spaces four channel bits long.

9. The storage disk of claim 4 wherein the address mark is made up of marks and spaces each having a length not equal to one-half the predetermined number of channel bits making up the data bits.

10. A storage media for use in a data storage system, comprising:

a storage substrate having a storage surface with a plurality of groove tracks and land tracks, the storage surface having a plurality of storage sectors for storing data with each storage sector comprising a header and a data storage field;

wherein the header is configured to have a plurality of repeated address blocks; and

wherein each of the plurality of address blocks comprise an address mark, an address field, and a error check field, the address field made up of a plurality of biphase cells to store a sector address in a biphase data format and the address mark made up of a distinct signal not found in the address field.

11. The storage media of claim 10 wherein the address blocks of adjacent tracks are written to both the land and groove tracks and are configured in a checkerboard format.

12. The storage media of claim 10 wherein only the land tracks are utilized and the address blocks of adjacent land tracks are written in a checkerboard format.

13. The storage media of claim 10 wherein only the groove tracks are utilized and the address blocks of adjacent groove tracks are written in a checkerboard format.

14. The storage media of claim 10 wherein each biphase cell is configured to have a mark-space or space-mark transition at a point in substantially the center of thereof.

15. The storage media of claim 14 wherein each biphase cell has a predetermine size comprising a predetermined number of channel bits.

16. The storage media of claim 15 wherein the predefined number of channel bits is six in length and the biphase cell includes a mark and a space, each being three channel bits in length.

17. The storage media of claim 15 wherein the predetermined number of channel bits is eight in length and the biphase call includes a mark and a space, each being four channel bits in length.

18. The storage media of claim 16 wherein the address bit comprises marks and spaces four channel bits in length.

19. The storage media of claim 14 wherein the address marks are made up of marks and spaces of a size not occurring in the biphase cell.

20. A method of configuring a storage media for robust addressing, comprising

defining a plurality of storage sectors on the storage media;

defining a header field with each storage sector; and

embossing a plurality of address blocks within the defined header field, each address block beginning with at least one address mark having a predetermined configuration, followed by an address field made up of a plurality of biphase cells, each biphase cell having a mark and a space with a transition in substantially the center thereof, the address block ending with an error detection code.

21. The method of claim 20 wherein each biphase cell is a predetermined number of channel bits long and the marks and space within each biphase cell each fill substantially one half of the biphase cell.

22. The method of claim 21 wherein the address marks are made up of marks and spaces having a dimension unequal to the marks and spaces within the biphase cells.

23. A robust optical data storage system, comprising:

a removable optical data storage medium having at least one storage surface with a plurality of predefined storage sectors thereon, each storage sector comprising a header region and a data storage region, the header region having a plurality of previously embossed address blocks thereon which are configured to be read asynchronously,

wherein each address block comprises an address mark, an address field and an error correction field, with the address field containing biphase coded address information and the address mark being a distinct pattern which does not occur in the address information;

a readout device positioned within the storage system for reading information from the optical storage medium; and

a decoding system for receiving information from the readout device and both recognizing the address mark and decoding the address information so as to identify the storage sector.

24. The system of claim 23 wherein the plurality of address blocks are arranged in a checkerboard manner.

25. The system of claim 23 wherein the decoding system includes an address mark recognition system and a data decoding system.

26. The system of claim 23 wherein each biphase cell is sized to include a predetermined number of channel bits.

27. The system of claim 26 wherein the predetermined number is 6.

28. The system of claim 26 wherein each biphase cell includes a level transition in substantially the center thereof.